Timer

→ The 555 timer is a highly stable device for generating accurate time delay or oscillation.

→ A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.

→ The 555 timer is versatile and easy to use in various applications. Various applications include oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator, burglar alarm, traffic light control and voltage monitor etc.

Description of Functional diagram

→ Fig gives the functional diagram for 555 IC timer.

→ In fig, three 5 kΩ internal resistors acts as voltage divider, providing bias voltage of $(2/3)V_{cc}$ to the upper comparator and $(\frac{1}{3})V_{cc}$ to the lower Comparator (LC), where V_{cc} is the supply voltage, since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval.

→ It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (Pin 5).

→ In applications, where no such modulation is intended, it is recommended by manufacturers that a capacitor (0.01 μF) be connected between control voltage terminal (Pin 5) and ground to by-pass noise or ripple from the supply.

→ Output of the Upper Comparator (UC) is applied to Reset (R) input of the flip-flop. Whenever the threshold voltage exceeds the control voltage, the output of the upper comparator goes high, and the output $\bar{Q}$ of the flip-flop (FF) is High.

→ A high output of $\bar{Q}$ from the flip-flop saturates the discharge transistor and discharge the capacitor connected externally to pin 7.

→ The complementary signal out of the flip-flop goes to pin 3 the output because of power amplifier is basically an inverter.

→ The output available at pin 3 is low. These conditions will pi until ~~comparator~~ Low Comparator (LC) triggers the flip-flop. L if the voltage at the threshold input falls below $+(2/3)V_{cc}$ i.e., Vc cannot cause the flip-flop to change again. It mea that the Vc can only force the flip-flop's output high of $\bar{Q}$.

→ To change the output of $\bar{Q}$ of flip-flop to low, the voltag at the trigger input must fall below $+(\frac{1}{3})V_{cc}$. When this occurs, LC triggers the flip-flop, forcing its output ~~of~~ of $\bar{Q}$ low.

→ The low output from the flip-flop turns the discharge transisto off and forces the power amplifier to output a high.

→ These conditions will continue, independent of the voltage on the trigger input. LC can only cause the flip-flop to output low.

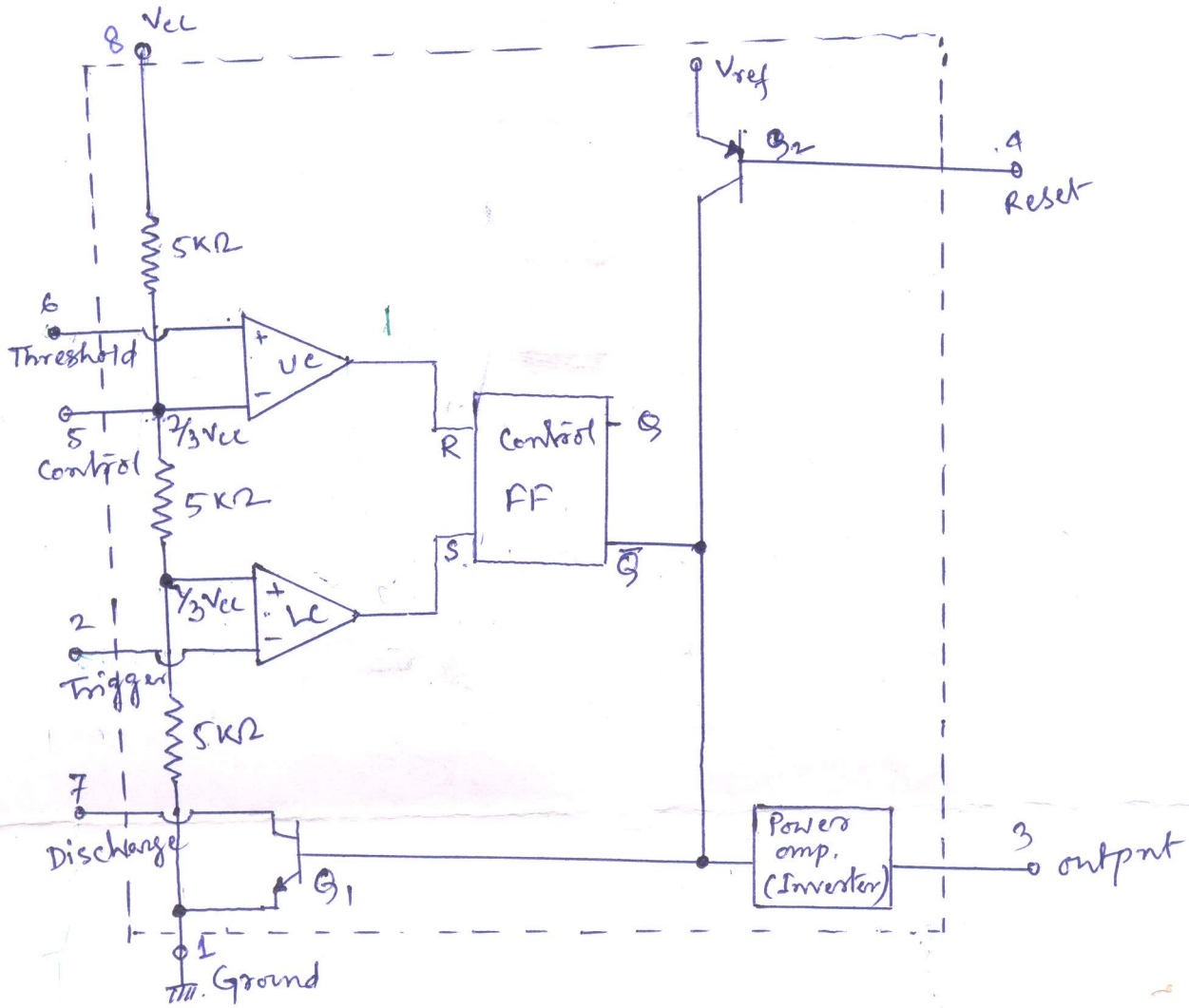
[Note: from the above discussion it is concluded that for the having low output from the timer 555, the on the threshold input must exceeds the control voltage or $+\frac{2}{3}V_{cc}$. The also turns the discharge transistor on. To force the output from the timer high, the voltage on the trigger input must drop below $+\frac{1}{3}V_{cc}$. This also turns the discharge transistor off.]

→ The reset input (Pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator (LC). This overriding reset is effective when the reset input is less than about 0.4V.

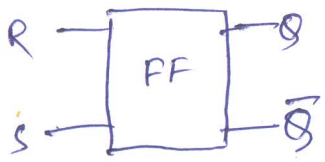
→ When this reset is not used, it is returned to V_{cc}.

→ The transistor Q_2 serves as a buffer to isolate the reset input from the FF and transistor Q_1.

→ The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{cc}.



Note



R	S	Q Q̄
0	0	Last value return / no change
0	1	1 0
1	0	0 1
1	1	undefined / Invalid

Monostable Operation

→ Fig shows a 555 timer connected for monostable operation.

→ In the standby (stable) state, the output $\bar{Q}$ of the control flip-flop is High that is FF holds transistor Q_1 on, thus clamping the external timing capacitor C to ground.

→ The output remains at ground potential, i.e. Low.

→ As the trigger passes through $V_{cc}/3$, the FF is set, i.e., $\bar{Q} = 0$. This makes the transistor Q_1 off and the short circuit across the timing capacitor C is released.

→ As $\bar{Q}$ is Low, output goes High ($= V_{cc}$).

→ The timing cycle now begins.

→ Since C is unclamped, voltage across it rises exponentially through R towards V_{cc} with a time constant RC.

→ After a time period T, the capacitor voltage is just greater than $(2/3)V_{cc}$ and the upper comparator resets the FF, that is, $R = 1, S = 0$ (assuming very small trigger pulse width).

→ This makes $\bar{Q} = 1$, transistor Q_1 goes on (i.e. saturation), thereby discharging the capacitor C rapidly to ground potential.

→ The output returns to the standby state or ground potential.

→ The voltage across the capacitor at any instant during charging is given as

$$v_c = V_{cc}(1 - e^{-T/RC})$$

Substituting $v_c = \frac{2}{3} V_{cc}$ in above eqn. we get the time taken by the capacitor to charge from 0 to $+\frac{2}{3}V_{cc}$

Therefore, $\frac{2}{3}V_{cc} = V_{cc}(1 - e^{-T/RC})$

$$T = -RC \ln(1/3)$$

$$T = 1.1\, RC \text{ (seconds)}. \quad \text{---} (1)$$

→ It is evident from eqⁿ (1) that the timing interval is independent of the supply voltage.

→ It may also be noted that once triggered, the output remains in the High state until time T elapses, which depends only upon R and C.

→ Any additional trigger pulse coming during this time will not change the output state.

→ However, if a negative going reset pulse as in fig is applied to the reset terminal (Pin 4) during the timing ~~cir~~ cycle, transistor Q_2 goes off, Q_1 becomes on and the external timing capacitor C is immediately discharged.

→ The output now will be as in fig.

→ It may be seen that the output of Q_2 is connected directly to the input of Q_1 so as to turn on Q_1 immediately and thereby avoid the propagation delay through the FF.

→ Now, even if the reset is released, the output will still remain Low until a negative going trigger pulse is again applied at pin 2.

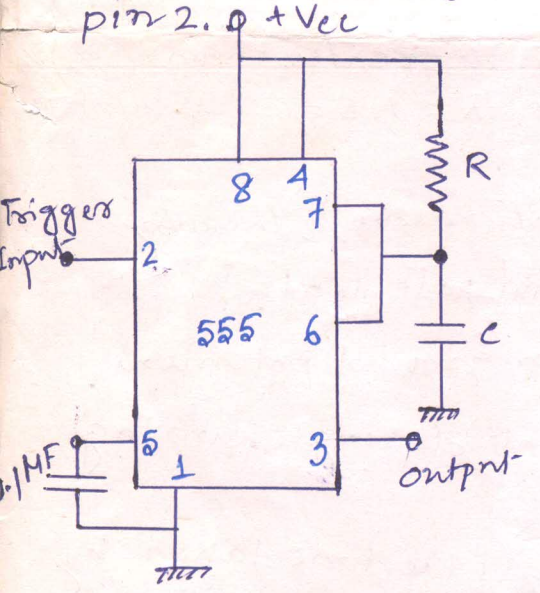


Fig:- Monostable multivibrator

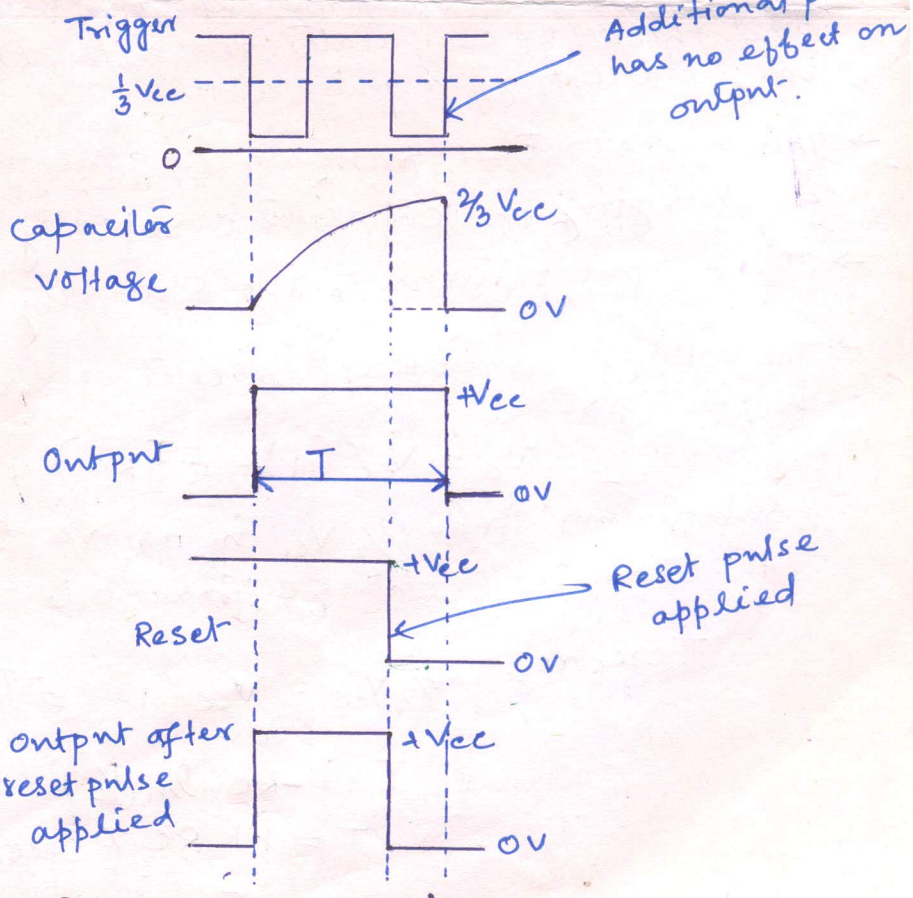


Fig:- Timing pulses.

Astable Operation

→ The device is connected for astable operation as shown in fig.

→ Comparing with monostable operation, the timing resistor is now split into two sections R_A and R_B.

→ Pin 7 of discharging transistor Q is connected to the junction of R_A and R_B.

→ When the power supply V_{cc} is connected, the external timing capacitor C ~~bar~~ charges towards V_{cc} with a time constant $(R_A + R_B)C$

→ During this time, output (Pin 3) is high (equal to V_{cc}) as Reset R = 0, set S = 1 and this combination makes $\bar{Q} = 0$ which has unclamped the timing capacitor C.

→ When the capacitor voltage equals (to be precise is just greater than) $\frac{2}{3}V_{cc}$ the upper comparator triggers the control flip-flop so that $\bar{Q} = 1$.

→ This, in turn, makes transistor Q_1 on and capacitor C starts discharging towards ground through R_B and transistor Q_1 with a time constant $R_B C$ (neglecting the forward resistance of Q_1).

→ Current also flows into transistor Q_1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q_1.

→ The minimum value of R_A is approximately equal to $V_{cc}/0.2$ where 0.2 is the maximum current through the on transistor Q_1.

→ During the discharge of the timing capacitor C, as it reaches (to be precise, is just less than) $V_{cc}/3$, the lower comparator is triggered and at this stage S = 1, R = 0, which turns $\bar{Q} = 0$. Now $\bar{Q} = 0$ unclamps the external timing capacitor C.

→ The capacitor C is thus periodically charged and discharged between $(\frac{2}{3})V_{cc}$ and $(\frac{1}{3})V_{cc}$ respectively.

→ Fig. shows the timing sequence and capacitor voltage waveform.

→ The length of time that the output remains High is the time for the capacitor to charge form $(\frac{1}{3})V_{cc}$ to $(\frac{2}{3})V_{cc}$.

→ It may be calculated as follows:

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{cc} volts is given by

$$v_c = V_{cc}(1 - e^{-T/RC})$$

The time T_1 taken by the circuit to change from 0 to $(2/3)V_{cc}$

$$(2/3)V_{cc} = V_{cc}(1 - e^{-T_1/RC})$$

or, $T_1 = 1.09\,RC$

and the time T_2 to change from 0 to $(1/3)V_{cc}$ is

$$(1/3)V_{cc} = V_{cc}(1 - e^{-T_2/RC})$$

or, $T_2 = 0.405\,RC$.

So, the time to change from $(1/3)V_{cc}$ to $(2/3)V_{cc}$ is

$$T_{HIGH} = T_1 - T_2 = 0.69\,RC$$

So, for the given circuit,

$$T_{HIGH} = 0.69\,(R_A + R_B)C.$$

The output is low while the capacitor discharges from $(2/3)V_{cc}$ to $(1/3)V_{cc}$ and the voltage across the capacitor is given by

$$(1/3)V_{cc} = (2/3)V_{cc}\,e^{-T/RC}$$

Solving, we get $T = 0.69RC$

So, for the given circuit, $T_{LOW} = 0.69\,R_BC$.

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, total time,

$$T = T_{HIGH} + T_{LOW}$$

or, $T = 0.69\,(R_A + 2R_B)C$

So, $$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

and Duty cycle, $$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100\%$$

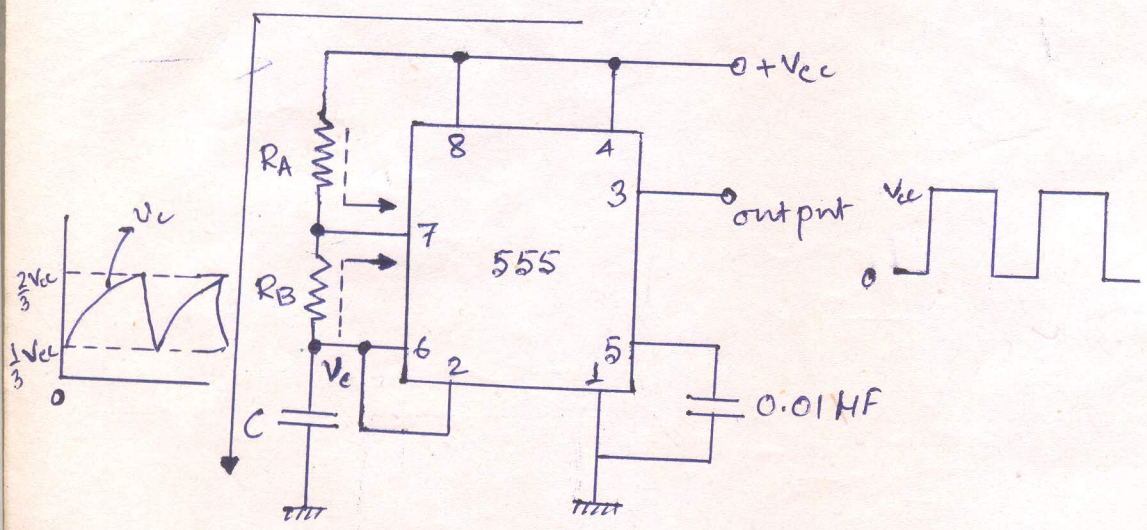


Fig:- Astable multivibrator using 555 timer.

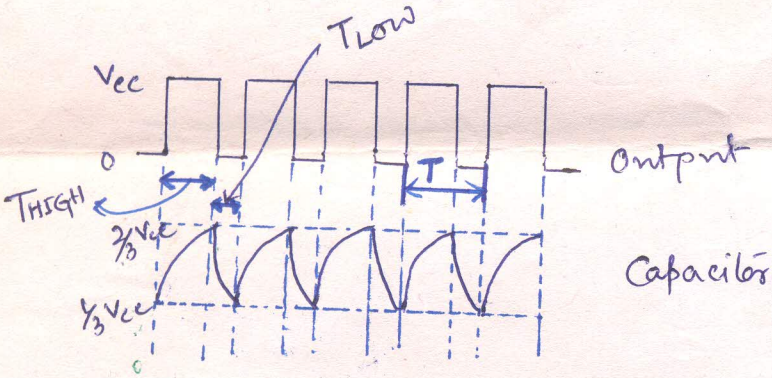


Fig: Timing sequence of astable multivibrator.